III. Amendments to the Specification

Please amend Paragraph 1 as follows:

[0001] This application is related to commonly-assigned, co-pending U.S. Patent Applications:

Serial No. 10/841,264 [[_____]], entitled "A Refresh Counter with Dynamic Tracking of Process, Voltage and Temperature Variation for Semiconductor Memory" filed on May 7, 2004 [[_____ (Attorney reference N1085-00179)]]; and

Serial No. 10/696,291, entitled "Circuit and Method for Self-Refresh of DRAM Cell Through Monitoring of Cell Leakage Current", filed on October 29, 2003, now U.S. Patent No. 6,862,239 ~~(Attorney reference: N1085-0212)~~, the contents of each being incorporated by reference herein.

Please amend Paragraph 6 as follows:

[0006] As noted, inactive cells exhibit leakage current from the access transistors and dielectric leakage current from the storage capacitors. The leakage current also depends, however, on the information stored in the memory bit cell, i.e., in the storage capacitor; that is, the leakage is different for memory cells holding binary "1" and binary "0". Normally, the leakage current of a single bit is too small for accurate detection. To measure the leakage current of a DRAM cell a large number of memory bit cells, e.g., ~~e.g.,~~ several thousand cells, are arranged in a structure and biased, as shown in FIGs. 1a and 1b with regard to n-channel and p-channel transistors, respectively. With regard to the monitoring array 100 of FIG. 1a, each dummy memory cell includes an n-channel transistor 110 and a corresponding storage capacitor 135 (labeled Cs). The transistor 110 can be applied a proper bias voltage on its gate to turn "on" or turn "off" the connection between the capacitor and the bit line. N-channel transistors 110 are electrically connected in parallel at corresponding source nodes 112 by a common bit line 120,

which may be set to a voltage referred to as VBL. The gate node 114 of each transistor 110 is connected to a common word line 125, which may be set to a voltage referred to as VSSB sufficient to turn transistors 110 off. Each drain node 116 of each transistor 110 is further connected to a substantially similar capacitor 135, each of which is connected to a common voltage plate 140. Common voltage plate 140 has a voltage, referred to as VCP, applied thereto. The drain node 116 of each transistor 110 is further electrically connected to a common extraction node 130 that allows for the measurement of an accumulated leakage from all coupled transistors 110 and capacitors 135.

Please amend the first paragraph of the "Brief Description of the Drawings" Section as follows:

[~~0001~~0011a] The accompanying drawings illustrate preferred embodiments of the invention, as well as other information pertinent to the disclosure, in which:

FIGs. 1a and 1b illustrate conventional current leakage detector circuitry for NMOS and PMOS type DRAMs, respectively;

FIGs. 2a and 2b illustrate an exemplary embodiment of current leakage detector circuitry in accordance with the principles of the present invention for PMOS and NMOS ~~NMOS and PMOS~~ logic, respectively;

FIGs. 3a and 3b illustrate a second exemplary embodiment of current leakage detector circuitry for PMOS and NMOS ~~NMOS and PMOS~~ logic, respectively; and

FIG. 4 illustrates an exemplary embodiment of a memory cell leakage monitor in accordance with the principles of the present invention for simultaneously monitoring leakage current in both programmed and unprogrammed cells.

Please amend paragraph 23 as follows:

[0023] FIG. 3b illustrates an embodiment 301 using similar current mirror configuration 320 associated with N-bit cells 310' of ~~p-channel~~ n-channel MOS (NMOS ~~PMOS~~) transistors TS. One skilled in the art would recognize that the operation of the current mirror in measuring extraction current in FIG. 3b is similar to that discussed with regard to FIG. 3a herein. Better approximation of the '1' state cells may be achieved by tuning VDDP to a higher voltage than VDD.

Please amend paragraph 25 as follows:

[0025] Although not shown, N-bit cells 210' and N-bit cells 310 may be substituted for N bit cells 210 and N bit cells 310', respectively, in an alternative DRAM configuration ~~comprising p-channel devices~~.